REMARKS

Claim Rejections Under 35 U.S.C. § 103

Claims 1-13 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Wright et al. (U.S. Patent No. 6,550,026). Applicant respectfully traverses.

Claim 1 recites, in part, "a first logic circuit for receiving data signals corresponding to a given bit location of each word of an output page of the memory device" and "a second logic circuit for receiving the data signals corresponding to the given bit location of each word of the output page." Claim 10 recites, in part, "a first logic circuit including a plurality of inputs coupled to receive data signals corresponding to a given bit location of each word of an output page of the memory device" and "a second logic circuit including a plurality of inputs coupled to receive the data signals corresponding to the given bit location of each word of the output page of the memory device."

Applicant notes that the Office Action has identified Wright et al.'s NOR gate 210 as corresponding to Applicant's first logic circuit and Wright et al.'s NAND gate 208 as corresponding to Applicant's second logic circuit. However, Wright et al.'s NOR gate 210 and NAND gate 208 are each coupled to receive either the even bits or the odd bits of a single data word or the even bits or odd bits of one data word plus one even or odd bit, respectively, of another data word. To compare multiple words, Wright et al. provides a given bit location to multiple first logic circuits. For example, to compare Wright et al.'s first data word and third data word, one NOR gate 210 would receive the even bits from the first data word while another NOR gate 210 would receive the even bits from the third data word along with one of the even bits from the first data word. *See, e.g.,* Wright et al., column 8, lines 35-48. Similar connections are utilized for the odd bits to NAND gates 208.

The Office Action asserts, "Thus, it would have been obvious to one skilled in this art that Wright et al also suggest the compression testing for a same given bit location across different words (of a memory array) altogether at the same time." Office Action, page 3, first paragraph. However, Applicant contends there is no teaching or suggestion to modify the circuitry of Wright et al. to utilize a single bit location for different words in its NOR gates 208 and NAND gates 210 while still addressing Wright et al.'s direction to provide even bits

or odd bits of one data word plus one even or odd bit, respectively, of another data word, to a set of its NOR gates 208 and NAND gates 210. Specifically, to read on Applicant's claim, one would have to ignore Wright et al.'s practice of providing one bit to multiple sets of its NOR gates 208 and NAND gates 210 as this one bit duplicates a bit location within the other set of NOR and NAND gates and, using the Office Action's modification, there is no set of NOR and NAND gates to which this one bit can duplicate. That is, if each set of NOR and NAND gates receives a given bit location, each set of NOR and NAND gates would be mutually exclusive with regard to bit location such that no bit location from any set of NOR and NAND gates would correspond to a bit location in any of the remaining NOR and NAND gates. Thus, it would require a modification of Wright et al.'s principle of operation in order to support rejection of claims 1 and 10. *See*, MPEP § 2143.01 (provides that if the proposed modification or combination of the prior art would change the principle of operation of the prior art invention being modified, then the teachings of the references are not sufficient to render the claims *prima facie* obvious).

In view of the foregoing, Applicant contends that Wright et al. does not teach or suggest at least these limitations of Applicant's claims 1 and 10. As claims 2-9 depend from and further define patentably distinct claim 1 and claims 11-13 depend from and further define patentably distinct claim 10, these claims are also believed to be allowable. Applicant thus respectfully requests reconsideration and withdrawal of the rejection under 35 U.S.C. § 103(a), and allowance of claims 1-13.

Allowable Subject Matter

Applicant acknowledges that claims 14-96 were indicated as being allowed.

CONCLUSION

Applicant believes that all of the pending claims are in condition for allowance and respectfully requests a Notice of Allowance be issued in this case. If the Examiner has any questions or concerns regarding this application, please contact the undersigned at (612) 312-2204.

Respectfully submitted,

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